

## INITIAL INFORMATION DATA SHEET

### APPLICATION INFORMATION

Application Type:: Regular  
Subject Matter:: Utility  
Title:: Low Jitter Clock for a Physical  
Media Access Sublayer on a Field  
Programmable Gate Array  
Docket Number:: X-1061US  
Request for Early Pub?:: No  
Request for Non-Pub?:: Yes  
Total Drawing Sheets:: Four  
Small Entity?:: No  
Petition included?:: No

### INVENTOR INFORMATION

Inventor Authority Type:: Inventor  
Primary Citizenship Ctry:: US  
Status:: Full Capacity  
Given Name:: Atul V.  
Family Name:: Ghia  
Street:: 5573 Ora Street  
City:: San Jose  
State or Province:: CA  
Postal or Zip Code:: 95129

Inventor Authority Type:: Inventor  
Primary Citizenship Ctry:: India  
Status:: Full Capacity  
Given Name:: Vasisht M.  
Family Name:: Vadi  
Street:: 630 Taylor Court, Apt. 10  
City:: Mountain View  
State or Province:: CA  
Postal or Zip Code:: 94043



[illegible]

Representative Customer Number::	24309	
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## ASSIGNEE INFORMATION

Assignee Name::	Xilinx, Inc.
Street::	2100 Logic Drive
City::	San Jose
State or Province::	California
Postal or Zip Code::	95124